METHOD FOR PRODUCING A CIRCUIT UNIT

~~A circuit unit and a method for producing a circuit unit~~

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates to a circuit unit comprising at least an insulating substrate on which a conductive coil is located, and an integrated circuit whose connection points are electrically connected with the coil ends. The invention relates further to a method for producing such a circuit unit.

2. RELATED TECHNOLOGY

Circuit units of the above type are known from the prior art, being designed for example as compact electronic modules which are inserted in chip cards for noncontacting data exchange with a terminal. For example US-PS 4,999,742 discloses a circuit unit in the form of an electronic module with an insulating substrate on which a ring-shaped wound coil is glued. The coil ends are guided into the receiving space arising through the ring-shaped coil, and electrically connected there with the connection points of an integrated circuit. The receiving space for the integrated circuit and coil ends is cast with a casting compound for protecting these sensitive components from mechanical loads.

The electronic module known from US-PS 4,999,742 has a compact structure but the coil must be wound in a separate method step and glued on the insulating substrate in a further method step.

However, the as yet unpublished German patent application P 44 16 697.4 discloses a circuit unit in the form of a chip card having printed on one card layer of the multilayer card body a coil from a conductive lacquer whose ends are electrically connected with the connection points of an integrated circuit.

The structure of the circuit unit known from patent application 44 16 697.4 has the advantage that the coil is printed directly on a card layer so that the method step of applying a separately manufactured coil to an insulating sub-

strate is omitted. For some applications of the circuit unit, however, it is desirable for the coil to have a higher number of turns than can be realized with the structure explained above. Furthermore it may be desirable to provide the circuit unit with relief embossing. One must then make sure the printed turns of the coil, which are generally formed as a very thin layer, are not interrupted. Also, the production method for the circuit unit should be further optimized with regard to inexpensive mass production.

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It is ~~therefore~~ the problem of the invention to further improve the abovementioned circuit unit and at the same time in particular to extend its range of applications. It is further the problem of the invention to propose a method for producing such a circuit unit.

BRIEF SUMMARY OF THE INVENTION

~~This problem is solved by the independent claims.~~ A

One advantage of the invention is to be seen in that a higher number of turns can be realized than on the structure known from German patent application 44 16 697.4. The coil A can still be applied directly to the substrate of the circuit unit so that an additional method step for applying a separately manufactured coil is unnecessary. This is made possible by the fact that coil layers and insulating layers are applied alternately to the insulating substrate, the individual coil layers being electrically interconnected via plated-through holes so as to yield a coil. The coil layers and insulating layers are preferably printed on. Alternatively it is also possible for the insulating layers to consist of thin insulating foils on which the coil layers are printed on one or both sides. The throughplating through the insulating layers can be done in the simplest case by providing windows or holes in the insulating layers through which the conductive material of the coil layers penetrates when the coil layers are printed on or the layers laminated together. Additional conductive material can likewise be applied for throughplating, or additional conductive elements provided.

A further advantage of the invention is to be seen in that the circuit unit can be manufactured especially easily by the multiple-copy method, since one can apply the coil layers and also the insulating layers (depending on the embodiment) using printing technology, with which multiple-copy production is commonplace.

Furthermore the invention has the advantage that the coil ends can be adapted especially easily to the various possibilities of forming the electric connection between the coil ends and the connection points of the integrated circuit.

Furthermore it is advantageous that the invention permits relief embossing of the circuit unit without restriction, with no danger of one or more turns of the coil being interrupted. For this purpose the turns of the coil are guided outside the relief embossing area of the circuit unit or between the individual relief embossing lines, whereby the width of the turns can be greater than the line spacing for compensating production tolerances, or the turns run in the area of the embossed characters but are wider than the character size.

BRIEF DESCRIPTION OF THE DRAWINGS

Some embodiments and further advantages of the invention will be explained in connection with the following figures, in which:

Fig. 1 shows a circuit unit in a plan view,

Fig. 2 shows a circuit unit in a perspective view,

Fig. 3 shows a cross section along line ~~A — A~~ III-III of Fig. 2,

Figs. 4, 5 show embodiments for contacting a coil with an integrated circuit or module,

Figs. 6 to 10 show embodiments for throughplating for forming an electric connection between opposite coil layers in cross section,

Fig. 11 shows a circuit unit with marked relief embossing fields in a plan view,

Figs. 12, 13 show embodiments for forming and arranging turns of a coil as an enlarged detail in a plan view.

DETAILED DESCRIPTON OF PREFERRED EMBOIMENTS OF THE INVENTION

Fig. 1 shows systematically a circuit unit in the form of a chip card for noncontacting data exchange in a plan view. The dimensions of such chip cards are identical with the dimensions of chip cards for contacting data exchange, which are fixed in ISO standard 7810. The circuit unit contains insulating substrate 1 in the form of a card layer on which coil 3 is located whose free ends 15 and 19 are electrically connected with the connection points of integrated circuit 7. The integrated circuit can also be cast into a module which, for easier contacting of integrated circuit 7, has contact surfaces which are electrically connected with the connection points of integrated circuit 7. The turns of coil 3 run along the outer edge of the card layer, yielding a large-area coil in the interests of high energy input.

Fig. 2 shows a perspective view not true to scale of an inventive circuit unit which is produced as described in the following. On insulating substrate 1, which exists e.g. in the form of a card layer (see Fig. 1) one first applies first coil layer Section 9, which is dash-lined in Fig. 2 and can contain a plurality of turns (coil layer Section 9 shown contains only one turn in order not to complicate the drawing). Coil layer Section 9 is preferably printed on with a conductive lacquer, but it is also possible to spray on the coil layer using a corresponding mask, or to etch it out of a conductive coating located on the substrate. Other production techniques are conceivable.

After applying coil layer Section 9 one applies to insulating substrate 1 insulating layer 11, which is hatched in Fig. 2 and covers the turns of coil layer Section 9. Insulating layer 11 has window 13 and is applied to coil layer Section 9 in such a way that first end 15 of coil layer Section 9 is not covered thereby and at least the Second end area of the last turn of coil layer Section 9 is accessible through window 13. Insulating layer 11 is preferably likewise printed on, but it is also possible here to spray it on using a corresponding mask or to use as insulating layer 11 a thin insulating foil, etc.

In a further method step one applies further coil layer Section 17 to insulating layer 11 using the same techniques as for applying coil layer Section 9. Further coil layer Section 17 is preferably also printed on. Coil layer Section 17 is electrically connected with coil layer 9 through window 13 in insulating layer 11, yielding coil 3 consisting of coil ~~layers~~ layer Section 9 and 17. One can facilitate the formation of an electric connection between coil ~~layers~~ layer Section 9 and 17 by making the coil ends which are electrically interconnected wider than the turns of the coil, as also shown in Fig. 2. It is easy to realize such widening by printing technology. Details on the connecting technique will be described below.

One can optionally repeat the application of further insulating layers and coil layers in the explained manner once or several times until circuit unit coil 3 composed of the coil ~~layers~~ layer Section has the desired number of turns. One must thereby make sure that first end 15 of the coil layer Section first printed on (e.g. layer 9) is not covered, and that the circuit unit does not exceed a predetermined height. When printing on the last coil layer Section (e.g. layer 17) one can overprint first end 15 of the first printed coil layer Section with a conductive lacquer again. One then obtains two freshly printed first coil ends 15 and 19 of the coil layer Sections which can be electrically connected with the integrated circuit especially easily. First end 19 of the last applied coil layer Section, i.e. coil layer Section 17 in Fig. 2, is applied in such a way that it is especially easy to form an electric connection first from coil ends 15 and 19 to integrated circuit 7. In the embodiment of the invention shown in Fig. 2 the coil layers and insulating layers are applied to insulating substrate 1 in a kind of frame. In the shown embodiment, coil Section ends 15 and 19 are guided into the interior of the frame onto insulating substrate 1. One avoids superimposition of turns in a coil layer Section by guiding the internal ~~end~~ First Ends of the particular coil layer~~s~~ into the part enclosed by the frame, as shown in Fig. 2.

By suitable choice of the coil ends which are electrically connected with the integrated circuit one can always

avoid superimposition of turns in a coil layer Section. For example, if coil end 19 is to be outside the frame the internal or Second end of coil layer Section 17 is connected with Second End of coil layer Section 9 (Figure3) and the external first end of coil layer 17 guided outward.

Alternatively it is also possible to apply an insulating layer Section with a window to the last coil layer, whose free first end is connected with the integrated circuit. Through the window the free coil end can then be guided over the coil layer Section in any direction, since no short-circuit can occur between the turns of the coil because of the covering insulating layer.

According to the embodiment of Fig. 2 one applies integrated circuit 7 to the noncovered part of insulating substrate 1, electrically connecting the connection points of the circuit with first ends 15 and 19 of the resulting coil e.g. by means of bonding wires 21. One can simplify the formation of the electric connections from integrated circuit 7 to coil ends 15 and 19 by making the coil ends wider than the individual turns of the coil. For this purpose one need only accordingly adapt the artwork or, if the coil layers sprayed on, the masks used. No separate method steps are thus necessary for producing widened coil ends.

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Fig. 3 shows a cross section along line ~~A — A~~ III-III of Fig. 2 to illustrate the sequence of layers. Coil layer Section 9 is applied to insulating substrate 1, being covered by insulating layer 11 containing window 13 through which further coil layer Section 17 is electrically connected with coil layer Section 9. Further insulating layers and coil layers can follow alternately.

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In a variant the connection between integrated circuit 7 and coil ends 15 and 19 is not formed via bonding wires but by directly mounting integrated circuit 7 on coil ends 15 and 19. For this purpose integrated circuit 7, or module 23 containing integrated circuit 7, can either be mounted on coil ends 15 and 19 already applied, or circuit 7 or module 23 is first inserted in substrate 1 and then overprinted with coil ends 15 and 19.

Figs. 4A and 4B show
~~Fig. 4 shows~~ cross sections of two embodiments of the inventive circuit unit wherein coil first ends 15 and 19 were first printed on substrate 1, and module 23 or integrated circuit 7 then mounted on coil ends 15 and 19. Module 23 or integrated circuit 7 can be mounted either directly after the printing operation or only after a short period of time in which the printed conductive lacquer dries at least partly.

Fig. 4a shows substrate 1 with printed coil ends 15 and 19 and module 23. Module 23 contains integrated circuit 7 which is coated by casting compound 8 and whose connection points 27 are electrically connected with contacts 25 of module 23 via bonding wires. Module 23 is mounted on coil ends 15 and 19 in such a way that contacts 25 of module 23 touch coil ends 15, 19. The arrangement shown in Fig. 4a can be covered by a cover foil not shown in the figures, which optionally contains a gap for module 23. In the embodiment shown in Fig. 4a, module 23 is mounted on coil ends 15 and 19 in such a way that casting compound 8 points away from coil ends 15 and 19. However it is also possible to mount the module turned by 180°. In this case one should provide a corresponding gap in substrate 1 for partly receiving casting compound 8. This variant is used in particular when a low overall height of the circuit unit is to be achieved.

Fig. 4b again shows substrate 1 with printed coil ends 15 and 19. Integrated circuit 7 is mounted on coil ends 15 and 19 in such a way that connection points 27 of integrated circuit 7 touch coil ends 15, 19. As in the embodiment of Fig. 4a, the structure shown in Fig. 4b can also be protected by a cover foil not shown, which can optionally contain a gap for integrated circuit 7.

Figs. 5A and 5B show
~~Fig. 5 shows~~ cross sections of two embodiments of the inventive circuit unit whereby module 23 or integrated circuit 7 is overprinted for contacting with coil ends 15 and 19.

In Fig. 5a module 23 is fit into substrate 1 in such a way that the surface of module 23 is flush with the surface

of substrate 1. Coil ends 15 and 19 printed on after insertion of module 23 in substrate 1 extend over the surface of module 23 so far that they partly cover contacts 25 of module 23 so as to form an electric connection between contacts 25 and coil ends 15 and 19.

In Fig. 5b integrated circuit 7, instead of module 23, is inserted into substrate 1 in such a way that the surface of integrated circuit 7 is flush with the surface of substrate 1 and connection points 27 of integrated circuit 7 point upward. Coil ends 15 and 19 are printed on substrate 1 in such a way that they extend over connection points 27 of integrated circuit 7. This forms an electric connection between connection points 27 and each coil end 15 and 19. For embedding integrated circuit 7 in substrate 1 one can either provide a corresponding gap, or press the chip into substrate 1 using heat and pressure.

Some variants for throughplating will now be described with which one can form electric connections between two coil layers or between a coil layer and connection point 27 of integrated circuit 7 or contact 25 of module 23 through insulating layer 11, for example a thin insulating foil.

Fig. 6 shows an embodiment of the inventive circuit unit in cross section, in which the throughplating takes place when the individual layers of the circuit unit are laminated together. One can see the sequence of layers of the circuit unit before the laminating process.

According to Fig. 6 substrate 1a with coil layer Section 17 and substrate 1b with coil layer Section 9 are separated from each other by insulating foil 11. Window 13 is provided in foil 11 by punching, piercing or by laser beam at a place where coil layer~~s~~ Section 9 and 17 are opposite each other. Lamination produces a ~~compound~~ composite from individual layers 1a, 1b and 11. Simultaneously the laminating process forms an electric connection between coil layer Section 9 and coil layer Section 17 through window 13. This can be supported by applying to at least one of coil layer~~s~~ Section 9 and 17 opposite window 13 a small portion of conductive adhe-

sive 29 which flows into window 13 during lamination, thereby forming an electric connection between coil layer~~s~~ Section 9 and 17.

Fig. 7 shows an embodiment of the inventive circuit unit in cross section, in which insulating foil 11 is printed with coil layer~~s~~ Section 9, 17 one on each side, with layer~~s~~ Section 9 and 17 partly overlapping. In the overlap area insulating foil 11 has one or more windows 13 which are produced for example by punching, piercing or by laser beam. When coil ~~layers~~ Sections 9 and 17 are printed on insulating foil 11 by the screen printing method, windows 13 are filled with the printing material, for example a conductive lacquer, thereby forming electric connections between Ends of coil ~~layers~~ Section 9 and 17.

Fig. 8 shows a further embodiment for throughplating. As in Fig. ~~8 coil layers~~ 7 ends of coil sections 9 and 17 are applied to the opposite sides of insulating foil 11 so that they partly overlap. In the overlap area at least one thin wire 31 is slipped in to penetrate the end of coil layer Section 17, insulating foil 11 and at least partly also the End of coil layer Section 9, thereby forming an electric connection between coil ~~layers~~ Sections 9 and 17. Wire 31 can also be fed completely through coil layer Section 9 and bent at its end by a suitable apparatus. To facilitate the feedthrough of wire 31 one can heat it in one variant of the embodiment.

Fig. 9 shows an embodiment in which coil layer~~s~~ Section 9 and 17 are first applied to the opposite sides of insulating foil 11. At least one window 13 is then provided in coil layer~~s~~ Section 9 and 17 and intermediate insulating foil 11, for example by punching, piercing or by laser beam, in the area where opposite Ends of coil layer~~s~~ Section 9 and 17 overlap. Window 13 is finally filled with conductive adhesive 33 and an electric connection thus formed between coil layer~~s~~ Section 9 and 17.

~~Fig. 10~~ Figs. 10A and 10B shows an embodiment in which an electric connection can be formed between Ends of coil layers Section 9 and 17 by means of connecting element 35.

Fig. 10a shows the sequence of layers of the circuit unit before the laminating process. Coil layer 9 is applied to substrate 1. Above substrate 1 there is insulating foil 11

which carries coil layer Section 17 and has window 13 in an area opposite coil layer Section 9 and adjacent coil layer Section 17. Connecting element 35 is disposed on auxiliary carrier foil 37 above window 13 and overlapping with coil layer Section 17. Connecting element 35 can consist for example of a thermally activable conductive adhesive.

Fig. 10b shows the layer structure from Fig. 10a after lamination. The layers shown in Fig. 10a can be joined into a compound under pressure and heat by means of a conventional laminating press. The laminating press die pressing against the top of the structure is formed so that connecting element 35 is pressed through window 13 against coil layer Section 9 and connects therewith during the laminating process. The other end of connecting element 35 is pressed against coil layer Section 17 and connects therewith. This forms an electric connection between coil layers Section 9 and 17. Auxiliary carrier foil 37 comes off connecting element 35 during lamination and is then removed.

In a variant of the invention one can omit window or windows 13 in insulating layer 11. In this variant there is no electric connection between the individual coil layer~~s~~ Sections. The coil layers Section are instead coupled capacitively. Capacitive coupling can also be used for coupling integrated circuit 7 with coil 3 so that an electric connection can likewise be omitted here.

A further aspect of the invention is that it eliminates restrictions that existed up to now with respect to relief-embossing a circuit unit containing coil 3. This can be done by various measures each applicable with both single-layer and multilayer coils 3.

Fig. 11 shows a circuit unit in a plan view, with dotted lines delimiting areas 37 and 38 within which relief embossing is admissible in chip cards according to ISO standard 7811. Relief embossing can be used for example to bring out letters and numbers or other characters. The embossed characters can be printed on a paper voucher with a suitable apparatus if required. However, embossing can damage coil 3.

Lower area 37 is especially problematic in terms of possible damage to turns of the coil, since coil 3 is generally required to have a large area and the turns therefore run close to the edge of the circuit unit.

Fig. 12 shows an enlarged detail of the circuit unit shown in Fig. 11 in a plan view. To prevent interruption of the turns of coil 3, turn 39 is disposed between relief embossing field 37 and the edge of substrate 1 in the embodiment according to Fig. 3. If there is enough room, several turns or even all turns of coil 3 can also run here. Since no embossing occurs in this area there is no danger of the turns of coil 3 being interrupted by the embossing process. With a multilayer coil the room becomes scarce at higher numbers of turns than with a single-layer coil, since not all turns have to be disposed side by side.

Turns 41 running in the area of relief embossing field 37 are so greatly widened that they are wider than the size of the characters embossed there. This ensures that turns 41 are not interrupted by the embossing process, even if the embossed characters would each sever a cross section of turns 41 corresponding to the character size. If there is not enough room for one or more turns 39 outside relief embossing field 37, all turns 41 can be guided through relief embossing field 37.

Fig. 13 likewise shows an enlarged detail of the circuit unit shown in Fig. 11 in a plan view. According to the embodiment shown in Fig. 13 the turns of coil 3 are guided either between relief embossing field 37 and the edge of the circuit unit (turn 39), or following the relief embossing lines or between the individual relief embossing lines (turns 43). Turns 43 running between the relief embossing lines or directly following the relief embossing lines are somewhat widened to compensate production tolerances. This ensures that at least a partial area of turns 43 runs on a surface which is not embossed so that there is no danger of turns 43 being interrupted. In the embodiment shown in Fig. 13 it also

depends on the exact dimension of the turns whether no turn at all, or at least one turn 39, can be guided past the relief embossing field, i.e. whether there is enough room for one or even for several turns 39 between relief embossing field 37 and the edge of the substrate. The turn variants shown in Figs. 12 and 13 can also be combined.

Besides the already outlined measures, others are also conceivable for preventing interruption of the turns of coil 3 by embossing. For example the properties of the coating material used for producing the turns can be adapted as greatly as possible to substrate 1 to which they are applied, so that the coating material does not crack and thus interrupt the turns during embossing. It is likewise conceivable to use as a coating material conductive plastics which are so elastic that they do not crack during embossing.

In the embodiments in which one or more turns 39 are guided between relief embossing field 37 and the edge of the circuit unit, the resistance of coil 3 might possibly assume inadmissibly high values since turns 39 must be very narrow due to the little room available. This problem can be counteracted by applying turns 39 in greater layer thicknesses, which can be done for example by multiple printing. It is likewise possible to reduce the resistance by widening turns 39 in the areas where enough room is available.

The circuit unit can be produced either in single piece production or via sheets or webs which are divided into individual circuit units at the end of production.

The described measures for improving the circuit unit, for example providing a multilayer coil structure whereby different throughplating variants are possible, permitting relief embossing of the circuit unit by suitably selecting the coil layer dimensions and pattern, optionally also material, and directly contacting the integrated circuit or module with the coil, can be used either singly or in combination.